Transformerless Single-Phase UPQC with Fractional Order PID Control For Improved Power Quality

Dr. S. Jagadish Kumar[1], N. Chandana[2]

[1]Associate Professor, Department of Electrical and Electronics Engineering, JNTUH University College of Engineering (Autonomous) Jagtial, Telangana, India.

[2] PG, M.Tech (Electrical Power Systems), Department of Electrical and Electronics Engineering, JNTUH University College of Engineering (Autonomous) Jagtial, Telangana, India.

Abstract: This study presents a transformerless single-phase unified power quality conditioner (UPQC) using a fractional-order proportional-integral-derivative (FOPID) controller to improve power quality in compliance with IEEE Std 1159-2019 and IEEE Std 519-2022. Conventional PI controllers' flexibility needed to handle severe voltage sags, swells, and nonlinear loads. To overcome this, the proposed FOPID controller leverages fractional calculus to achieve faster transient response and superior disturbance rejection. Additionally, the transformer less modelling minimizes hardware volume and losses, while a standby converter lowers operational power consumption. MATLAB simulations confirm that the FOPID-controlled UPQC minimizes DC-link voltage ripple and total harmonic distortion (THD) effectively compared to traditional topologies.

Keywords: Fractional-Order PID (FOPID) Controller, Power Quality Enhancement, Nonlinear Load Compensation, Total harmonic distortion (THD).

I. INTRODUCTION

There has been a lot of research into different topologies of AC-DC, DC-AC, and AC-DC-AC converters, but much of it has focused on power quality (PQ) issues, such spikes, voltage dips, and harmonic distortions [1-4]. Dynamic voltage restorers (DVRs) [7], active power filters (APFs) [6] for series or shunt, or universal power quality conditioners (UPQCs) [5] dominate converter-based systems. Because of its small size, high performance, and cheap cost, UPQCs stand out among these systems [8], [9]. They can also offer series and shunt compensation with a single DC connection.

Two voltage source inductors (VSIs) and a line-frequency transformer (LFT) make up the conventional four-leg UPQC configuration, which is often used in single-phase settings [10]. Because it increases system size, weight, and cost, LFT is not suitable for low-power applications. Because of these restrictions, three-leg UPQC systems without transformers have been developed [11]. Modern topologies are more space-and power-efficient than their predecessors because to a reduction in the number of semiconductor devices and the elimination of circulating currents. Several different kinds of three-leg converters and methods for decoupling have been proposed [12–14] to enhance compensation performance.

Unfortunately, the three-leg UPQC design still isn't ready for voltage swell correction, even with these upgrades. A DC-link voltage higher than the grid voltage is necessary for its operation due to its efficiency being very load dependent. This dependency leads to a decrease in the modulation index under rated conditions, which in turn leads to an increase in harmonic distortion and semiconductor losses. Some have proposed hybrid topologies combining three-leg and two-leg converters as a solution to these issues [15]. These solutions enhance the ability to adjust voltage swells, but they reduce system efficiency since the auxiliary two-leg converter is always operating.

Beyond the structural and topological challenges, the control system plays a vital role in determining the dynamic performance of the UPQC. Conventional three-leg UPQC topologies heavily

rely on traditional Proportional-Integral (PI) controllers for DC-link voltage regulation and reference current tracking. However, PI controllers possess a rigid structure with fixed gains, making them highly sensitive to parameter variations, grid disturbances, and highly nonlinear loads. Under severe voltage sag, swell, or transient load conditions, standard PI control often exhibits sluggish transient responses, high overshoots, and an inability to adequately suppress harmonic distortion.

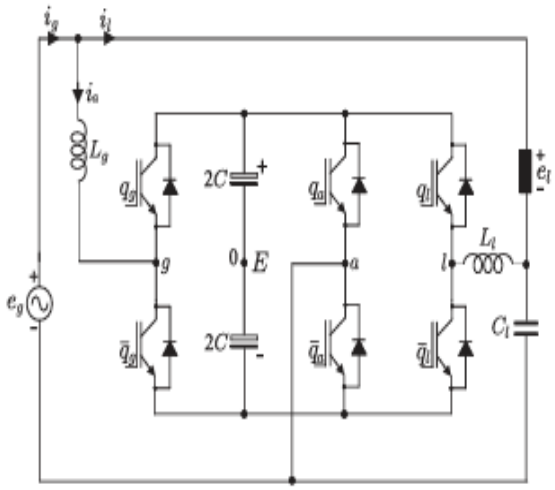

Fig. 1 Conventional single-phase three-leg converter (3L-UPQC)

Standard 3L-UPQC system shown in Fig.1 is used to fix power issues in a single-phase grid. It uses a three-leg switch setup instead of two completely separate full-bridge converters. The central, third leg is shared between both the series side and the shunt side. A number of decoupling techniques have been developed to prevent the modulation index from dropping during voltage spikes and to allow for high-modulation-index operation in rated and sag scenarios [16].

The control complexity rises when dealing with highly inductive loads or circumstances with a high degree of transient complexity, even if these approaches are still load-dependent. Combining a three-leg converter with an additional shunt converter is another approach that has been studied; this should enhance performance in both low-voltage and high-current scenarios [17]. But the process makes passive components bigger, which means the system isn't as compact. In response to these problems, this research introduces a novel decoupling method based on a standby converter and a three-leg UPQC. Along with improving voltage swell control capabilities and eliminating dependency on load factors, the proposed concept brings high modulation index operating under rated and voltage sag scenarios within reach. A less complicated method of standby control exists for controlling the DC-link voltage of the auxiliary converter; this method reduces power consumption and voltage ripple while maintaining a high level of system efficiency.

The following fields are primarily aided by this endeavor: One modern method for decoupling shunt and series units that doesn't rely on load characteristics is to connect the grid voltage to the shunt-side inductor filter (L_g). Power loss distribution, harmonic performance, and passive component modelling are just a few of the many topics covered in a comprehensive, full-scale research conducted under steady-state circumstances. A comparison of the proposed configuration to existing UPQC topologies demonstrating its superior performance. Extensive computer modelling and testing results confirm the system's feasibility and effectiveness.

II. SYSTEM TOPOLOGY

A) Introduction to the Circuit

A transformer less single-phase UPQC, the SB-3LG-UPQC is based on three-leg and standby converters, as seen in Figure 2(a). E_l and e_g are the single-phase grid and load voltages, C_s and C are the two direct current connections, L_g, C_l, and L_l are the inductor and capacitor filters, and a three-leg module are also part of the system. When $j = \{s_1, s_2, g, a, l\}$, the sets $q_j - q_j$ cannot coexist. If the switch is closed, then

$q_j = 1$, and if it is open, then $q_j = 0$. This indicates the state of the switching conduction. The suggested arrangement's simplified equivalent circuit is shown in Figure 2(b). Combines a full-bridge Standby Converter (shaded left block) with a core Three-Leg Module to overcome conventional limitations. By defining these dynamic voltage vectors independently, the standby converter can remain entirely inactive during normal grid operations to minimize losses, activating only during severe swells. Ultimately, this mathematical framework establishes the exact loop equations required to implement the external FOPID controller for optimized power quality correction.

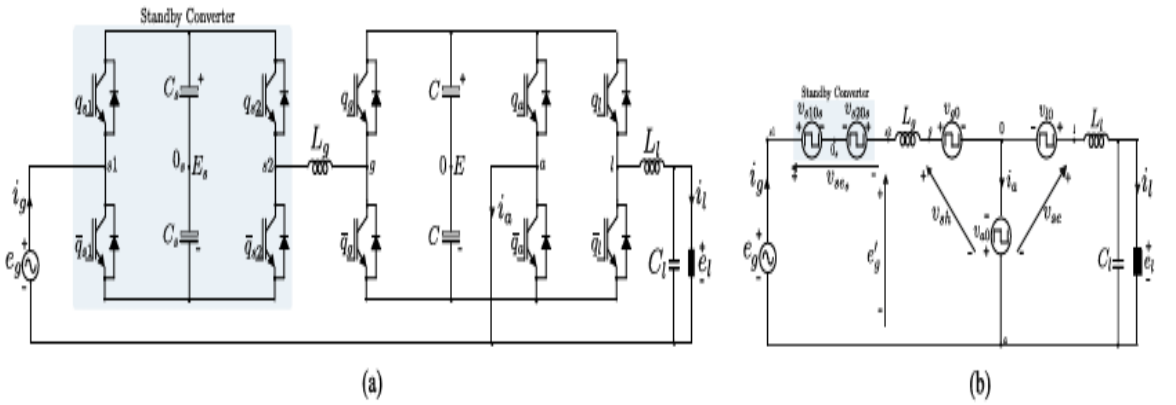

Fig.2 a) Single-phase ac-dc-ac SB-3LG-UPQC Converter. (b) An analogous circuit that has been simplified.

The following equations from Kirchhoff's rules of voltage and current:

$$Vse_s = e_g - e^1_g, \quad (1)$$

$$V_{sh} = e^1_g - Z_g\, i_g\,, \quad (2)$$

$$V_{se} = e_l + Z_l\, i_l, \quad (3)$$

$$I_a = i_g - i_l\,, \quad (4)$$

In a three-leg module, e_g' is the input voltage, V_{sh} is the shunt voltage, and Vse_s is the series converter voltage. The grid current is ig, the load current is i_l, and the shunt compensation current is i_a. The inductor filter L_l has an impedance of $Z_l = r_l + d/dt\ l_l$, whereas the inductor filter Lg has an impedance of $Z_g = r_g + d/dt\ l_g$. The values of Vse_s, V_{sh}, and V_{se} are obtained by taking into account the voltages at the converter poles:

$$Vse_s = V_{s10s} - V_{s20s} \quad (5)$$

When the system is operating properly, the proposed SB-3LG-UPQC might ensure that the standby converter is not activated, hence providing the necessary pole voltages for series and shunt compensation. The suggested architecture and control technique are shown to be resilient, efficient, and flexible by this behavior.

$$V_{sh} = V_{g0} - V_{a0} \quad (6)$$

$$V_{se} = V_{10} - V_{a0} \quad (7)$$

For two-leg modules, the converter's pole voltages may be expressed as vs10s, vs20s, vg0, vl0, and va0, respectively.

$$V_{j0s} = (2q_j - 1)\, E_s/2 \quad (8)$$

$$V_{j0} = (2q_j - 1)\, E_s/2 \quad (9)$$

where E represents the three-leg converter's dc-link voltage and Es represents the two-leg converters.

III. PWM STRATEGY

In this work, we present the SB-3LG-UPQC and outline two PWM control schemes for it. Section A: A Three-Leg Inverter with a Secondary Power Output Here we see how to use pulse width modulation (PWM) to deal with cases when the grid voltage drops below its rated level. The three-legged module regulates the grid's voltage and current in both cases. We may somewhat isolate the two modules' PWM techniques by following this path. So, it's necessary to come up with the PWM approach for the three-leg module separately first. The three-leg converter is managed by means of scalar pulse width modulation. The control strategy determines the reference pole voltages of the three-leg module, supposing that the reference voltages for the series and shunt are likewise supplied.

$$V^*_{l0} - V^*_{a0} = V^*_{se} \quad (10)$$

$$V^*_{g0} - V^*_{a0} = V^*_{sh} \quad (11)$$

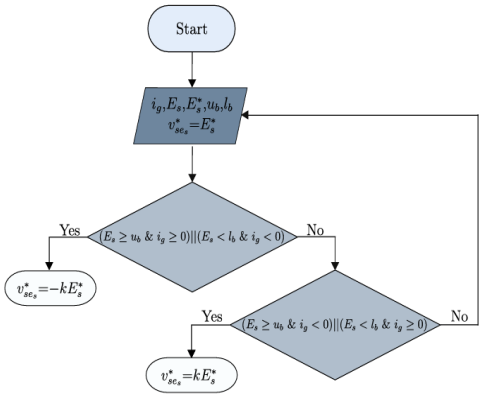

Fig.3 Flowchart for the regulation of Es in the standby operation.

Knowing v^*_{a0} allows one to solve these equations for v^*_{l0} and $v^*_{g0,}$ since the reference voltages v^*_{sh} and v^*se are specified by the series and shunt controllers, respectively. Hence, by rewriting equations (10) and (11) with the inclusion of an auxiliary variable ($v^*\mu$), they may be used.

$$V^*_{10} = V^*_{se} + V^*_{\mu} \quad (12)$$

$$V^*_{g0} = V^*_{se} + V^*_{\mu} \quad (13)$$

$$V^*_{a0} = V^*_{\mu} \quad (14)$$

In order to provide the following limits for the reference pole voltages, it is essential to get the auxiliary variable:

$$-E^*/2 \le V^* \le E^*/2 \quad (15)$$

It is necessary to meet the requirement (15) for the three-leg converter to function inside its linear domain. Following these calculations, where μ is the general apportioning factor, the reference voltage v^*_{μ} may be normalised in this context:

$$V_u{}^* = \mu V^*_{max} + (1-\mu) V^*_{min} \quad (16)$$

Where,

$$V^*max = E^*/2 - max \{V^*_{se}, V^*_{sh}, 0\} \quad (17)$$

$$V^*min = -E^*/2 - min \{V^*_{se}, V^*_{sh}, 0\} \quad (18)$$

There are switching losses because the reference pole voltages do not flip for extended periods of time when V= 0 or V= 1. Using the apportioning factor V to reduce these intervals will improve the converter's performance. It is possible that total harmonic distortion (THD) may be improved by adjusting V to 0.5. By controlling the dc-link voltage Es, the two-leg module may keep its power consumption to a minimum when in sleep mode. The components of a hysteresis voltage regulator are as follows: the grid current i_g, the reference voltage $E^*_{s,}$ and the bands representing the upper and lower hysteresis, μ_b and l_b, respectively, which are equal to $E^*_s +$ and $E^*_s - \gamma$) are all present. Figure 4 is a flow diagram depicting the process for handling Es. The initial clamping of legs s_1 and s_2 is clearly shown by the above equation ($V^*_{s10s} = V^*_{s20s} = E^*_s/2$). The pulse width is guided by the proportion of v^*s_{es} (kE^*_s) while the dc-link voltage E_s is being charged or discharged. Consequently, the following may be said about the voltages at the two-leg module's reference poles:

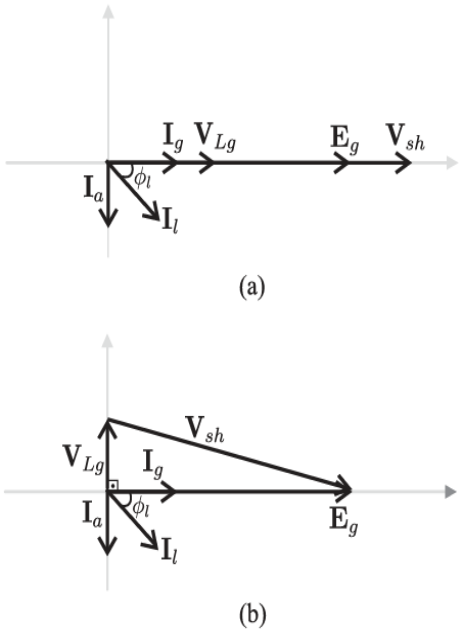

Fig.4 A phasor graph under rated conditions. (a) With respect to the typical 3L-UPQC. c) With reference to the proposed SB-3LG-UPQC.

$$V^*_{s10s} = - V^*se_s/2 \quad (19)$$

$$V^*_{s20s} = - V^*se_s/2 \quad (20)$$

The reference voltage V^*_{sh} of the three-leg module is impacted by the two-leg module's switch. This influence may only be taken into consideration by modifying the reference pole voltage V^*_{g0}, which is defined as $V^*_{g0} - V^*se_{s.}$ Pulse width modulation (PWM) is a standard technique that uses carriers to specify the states of the switches. Figure 3 shows

how the reference voltages generated by the proposed technique work. The hysteresis bands may be purposefully narrow in this mode of operation since legs s_1 and s_2 are employed purely to regulate Es and do not contribute to the fundamental frequency. Because ripple current stress is the primary cause of the capacitor's sluggish degradation over time, this effectively increases the capacitor's lifespan [19]. Active series filters work as follows: B. The efficiency and harmonic distortion of a three-leg converter in both rated and sag conditions are affected by its modulation index, which is particularly important for reducing grid voltage spikes in a shared-leg system. Under certain conditions, the proposed SB-3LG-UPQC's two-leg module swaps modes, allowing for series compensation and low modulation index operation. If a voltage spike were to start, the two-legged module would activate as an open-loop filter in series. When this strategy is used, the formula for v^*_{ses} is $E_g - e^*_g$.

$$V^*_{s10s} = V^*se_s + V^*_{s20s} \quad (21)$$

$$V^*_{s10s} = V^*se_s + V^*\mu_{sb} \quad (22)$$

$$V^*_s20s + V^*\mu_{sb} \quad (23)$$

IV. DC -LINK VOLTAGE REQUIREMENT

Both the 3L-UPQC and the SB-3LG-UPQC take the amplitude of the series and shunt converter voltages into account when determining the necessary dc-link voltage for the three-leg module. In both cases, the structure's series side is shown by

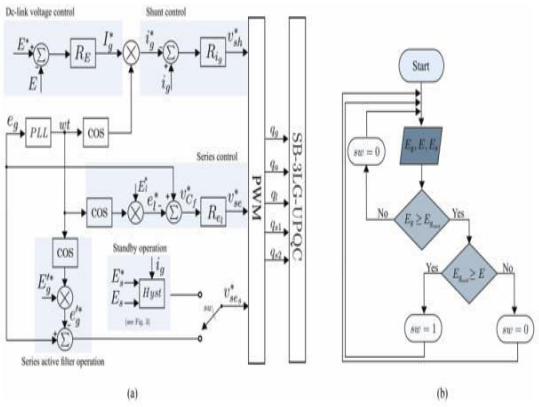

Fig. 5 (a) A schematic showing how the shunt and reference voltages in series are generated.

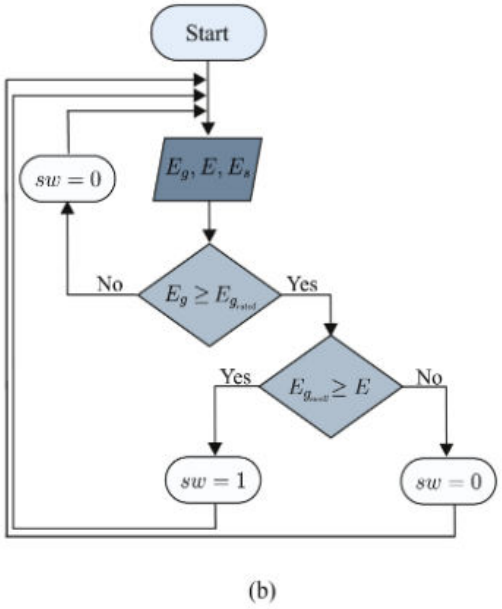

Fig.5 (b) A schematic of the s_w process.

Utilisation of this technology will reduce grid power disruptions. As can be seen in the phasor diagrams of Figure 5, the two systems use the shunt converter with distinct specifications. The converter voltage on the shunt side of the classic 3L-UPQC is determined by the shunt compensation current, which is frequently exactly proportional to the reactive and harmonic power (Figure 5 (b)).

TABLE 1
PARAMETERS FOR SIMULATION TESTS

Parameter	Symbol	Value
Grid Voltage	eg	110Vrms, 77Vrms, 165 V rms
Load reference Voltage	e^*_l	110V rms
Switching frequency	fs	10KHZ
Dc-link capacitor	C	2.2 mF
Three- leg shunt inductance	Lg	5mH
Series filter inductance	L_l	2mH
Series filter capacitance	C_l	18μF

RL Load:

Parameter	Symbol	Value
DC – link voltage	E, Es	170V
Load power factor	Cos (δ1)	0.72(lagging)
Apparent power	S1	0.75KVA

Non-Linear Load:

Parameter	Symbol	Value
DC- link voltage	E, E_s	170V
Load resistance	R_k	22.5/15Ω
Apparent power	S_1	0.8/1.6KVA
Load filter capacitance	C_k	2.2mF
Load filter inductance	L_k	7mH

V. FOPID CONTROLLER

Classical Proportional-Integral (PI) controllers are extensively used in the current converter control design due to its simplicity, ease of construction, and effective reduction of steady-state errors. When dealing with mode transitions and bidirectional energy transfer, multiport power converters often encounter nonlinearities. Some further constraints of PI controllers include their large working range and high dynamic response requirements. According to the study's findings, a Fractional Order PID (FOPID) controller would be a better fit for the control loops of the converter system than the traditional PI controller. A standard FOPID controller's transfer function is written as:

$$C(s) = K_p + \frac{Ki}{s\lambda} + K_d s^{\mu} \qquad (24)$$

Where:
Profitability as a function of input K_p, K_i Decrease in loss. K_d Profit from product derivatives where λ is an integral with values between zero and one. where μ ranges from zero to one. By including the tuning knobs λ and ν, which provide enhanced command over the phase and gain margins, the system's stability and band width are enhanced. A FOPID controller's block diagram is shown in fig 6. This modified version of the conventional PID controller uses fractional expressions for the integral and derivative commands rather than integers. fractional parameters provide independent control over the system's frequency response, allowing researchers to optimize the phase margin and gain margin more precisely without altering the main loop gains.
By controlling the phase delays during the PWM carrier wave generation, the FOPID controller ensures cleaner voltage injection, minimizing the ripple content delivered to the final non-linear load block.

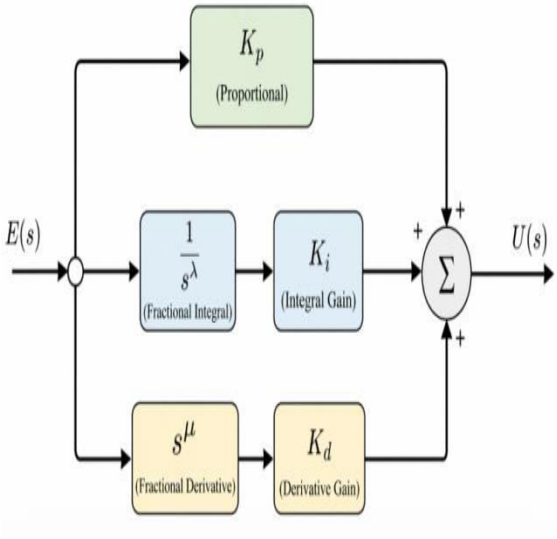

Fig.6 FOPID controller-based closed-loop process control system.

The FOPID controller enhances the charger's stability, power quality, and flexibility; it is used by the three-mode multiport EV charger. With this controller upgrade, it transforms from a simple power conversion unit into an intelligent, versatile, and grid-compliant energy distribution system that can function in both urban and rural areas. You should choose it if efficiency and reliability are your top priorities.

VI. SIMULATION CIRCUIT

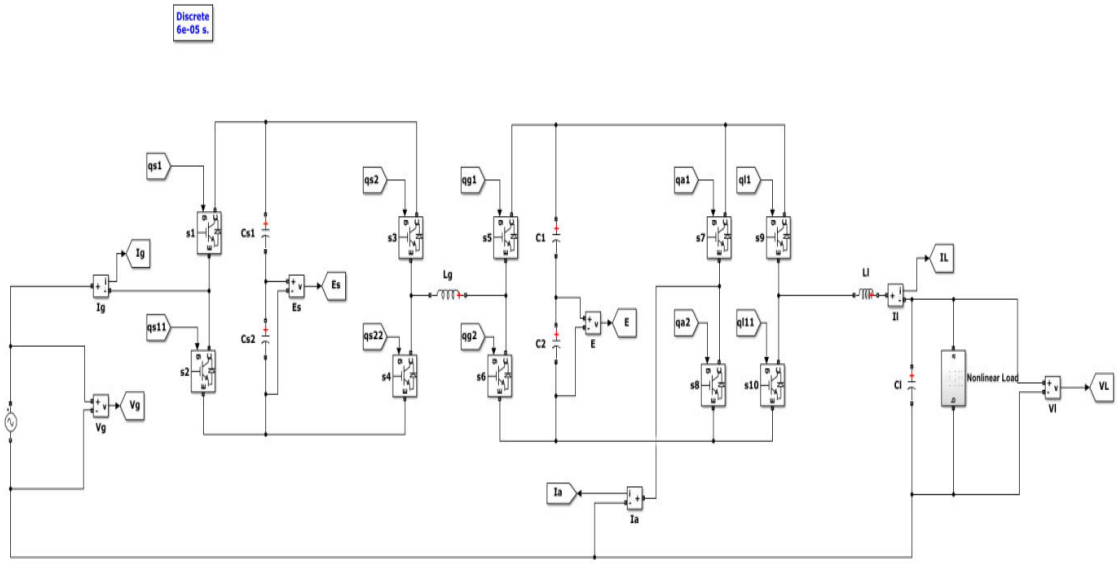

Fig.7. FOPID Controlled SB-3LG-UPQC single-phase ac-dc-ac converter's MATLAB/SIMULINK circuit.

The above fig.7 MATLAB/Simulink circuit model represents a single-phase AC-DC-AC converter integrated into a Fractional-Order PID (FOPID) controlled Split-Bus 3-Leg Unified Power Quality Conditioner (SB-3LG-UPQC). The grid-side AC voltage and current enter from the far left, passing into a shunt active power filter stage controlled by semiconductor switches s_1 to s_4. This shunt stage works with the split DC-link capacitors Cs_1 and Cs_2 to actively inject compensating currents that eliminate current harmonics and reactive power caused by the nonlinear load.

The system bridges energy through a central interface featuring inductor L_g and switches qg1 and qg_2 into the main split DC-bus capacitors C_1 and C_2. These main capacitors feed a series active power filter stage constructed from full-bridge inverter switches S_7 to S_{10}. This series inverter injects dynamic compensation voltages into the transmission line to eliminate supply-side voltage sags and swells. An LC low-pass filter consisting of inductor L_l and capacitor C_l then smooths out high-frequency switching ripples. Finally, the stabilized AC power reaches the nonlinear load, regulated continuously by the FOPID controller to ensure fast tracking, low total harmonic distortion, and robust voltage profiles.

A. RESULTS WITH PI CONTROLLER

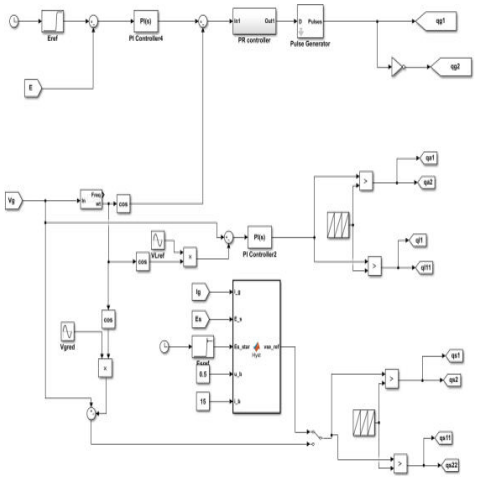

Fig.8 Control system

The above fig.8 shows closed-loop control system using PI and PR regulators to generate converter switching pulses. At the top, the error between the reference voltage and actual DC voltage is calculated. This error passes through PI Controller to maintain active power balance. The output then enters a Proportional Resonant (PR) controller to eliminate tracking errors at grid frequency. A pulse generator block converts this signal into complementary gating pulses.

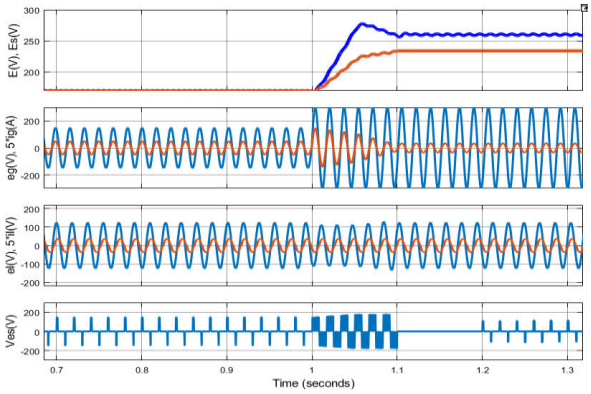

Fig.9. Vacuum swell temporary results in models. A 50% spike in grid voltage causes an interruption in power flow.

The above Fig.9 shows The un optimized baseline control setup results in a severe transient overshoot in the DC-link voltage (≈ 280) and temporary tracking distortion in the grid current waveform.

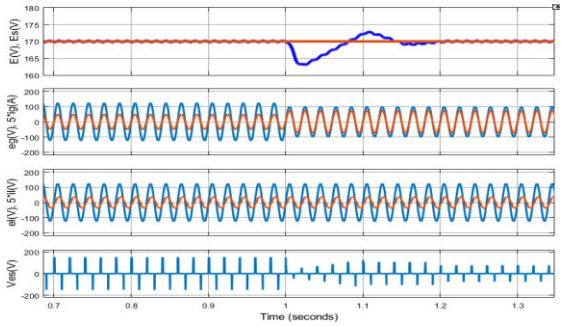

Fig.10. The simulation's brief vacuum drooping is to be expected. A 30% drop in grid voltage is the culprit behind the transient.

Voltage Dip: Fig.10 drops heavily to 163V. In Current Transition it shows minor settling ripple. Load Protection: Both plots achieve perfect isolation, keeping the load voltage completely stable.

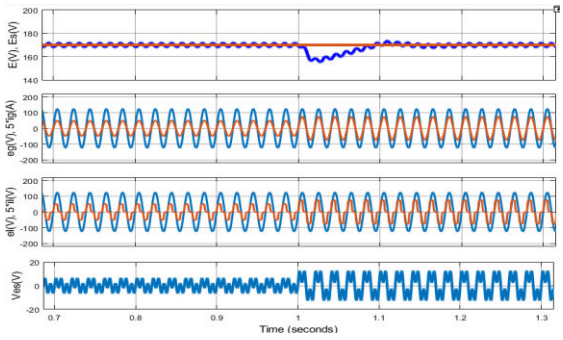

Fig.11. Results obtained from the model after changes to the load power. There is a transient when the load power goes from 0.8 kVA to 1.6 kVA.

The above fig.11 shows simulation waveforms demonstrate the system's rapid transient recovery when the load power steps up from 0.8 kVA to 1.6 kVA at1 second. The main DC-link voltage experiences a minor momentary dip before stably recovering within 0.1 seconds under FOPID control, while the grid and load current amplitudes seamlessly scale up while keeping the load voltage completely undistorted.

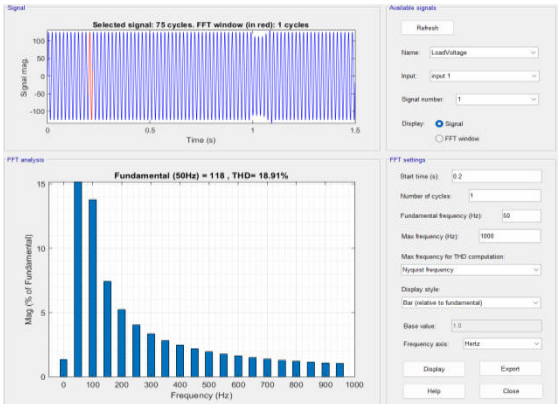

FIG.12 THD% Load Voltage

Total Harmonic Distortion (THD) Figure.12 it exhibits a very high distortion of 18.91%. Fundamental Magnitude (50Hz) The peak value of the fundamental component is 118. which represents the primary sinusoidal voltage or current wave delivered by the source. While this fundamental peak of 118 carries the actual real power intended for the load, the surrounding 18.91% harmonic distortion.

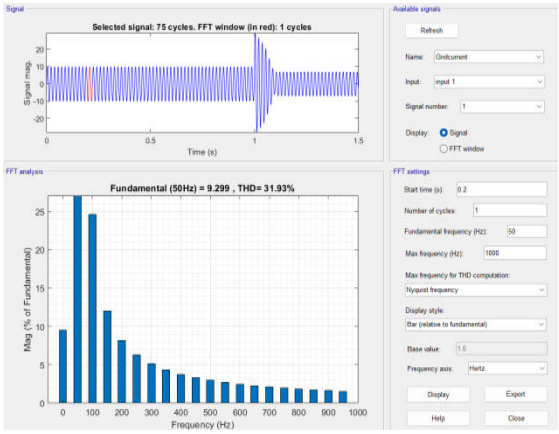

Fig.13 THD% Grid Current

The above fig.13 Shows Critical distortion at 31.93%. Fundamental Magnitude (50Hz) The peak value increases 9.299.

B) RESULTS WITH FOPID CONTROLLER

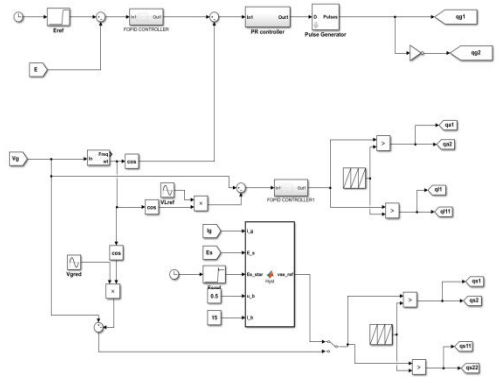

Fig.14 Control system with FOPID Controller

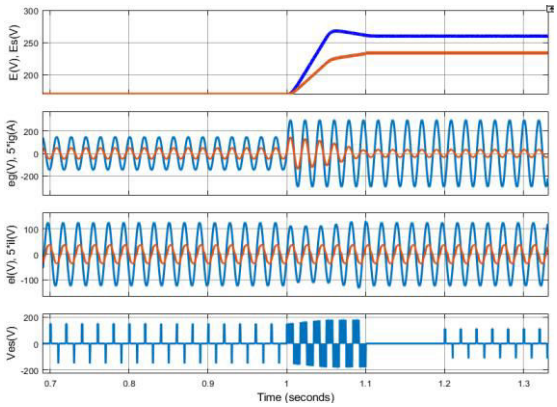

Fig.15 Vacuum swell transient outcome in simulations. Interrupting power surge due to a 50% increase in grid voltage.

The above fig.15 shows the optimized controller eliminates the DC voltage overshoot entirely and enables a seamless grid current transition, minimizing systemic electrical stress and maximizing stability.

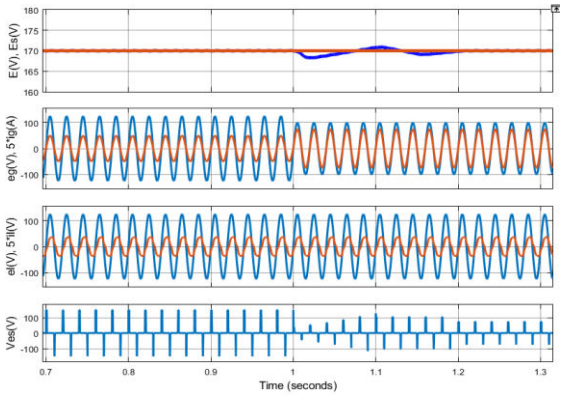

Fig. 16. Vacuum sag transient outcome from simulation. A 30% drop in grid voltage causes the transient.

The above Fig. 16 represents the dampens the drop tightly to 168V. And it is tracking is immediate and seamless. maintains clean, uniform switching.

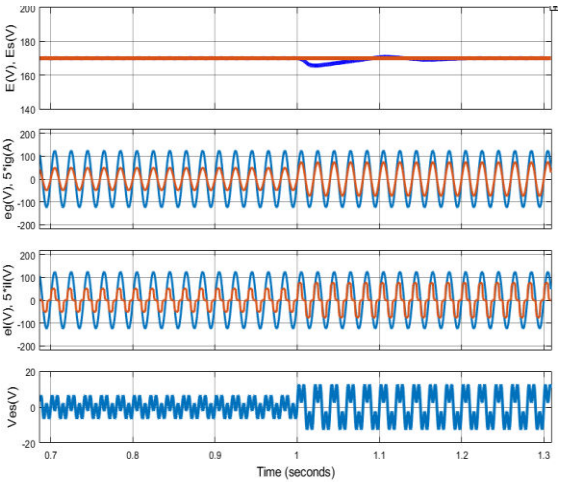

Fig. 17. Findings from the simulation after varying the load power. An increase in the load power from 0.8kVA to 1.6kVA causes a transient.

The above fig.17 demonstrates that under FOPID control, the step increases in load power at t=1.0 sec causes an exceptionally minor transient dip in the DC-link voltage with near-instantaneous recovery. Concurrently, the grid, load, and common-leg currents increase in amplitude while maintaining perfectly stable, undistorted terminal voltage profiles.

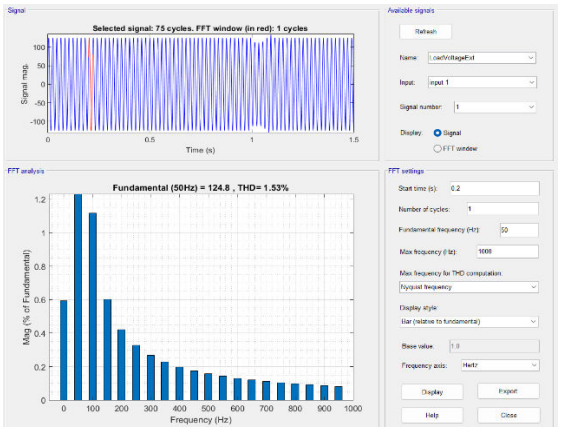

FIG.18 THD% Load Voltage

The above fig.18 shows a much cleaner signal with a significantly lower THD of 1.53%. Fundamental Magnitude (50Hz) The peak value of the fundamental component is 124.8. It indicating an improved delivery of useful active current.

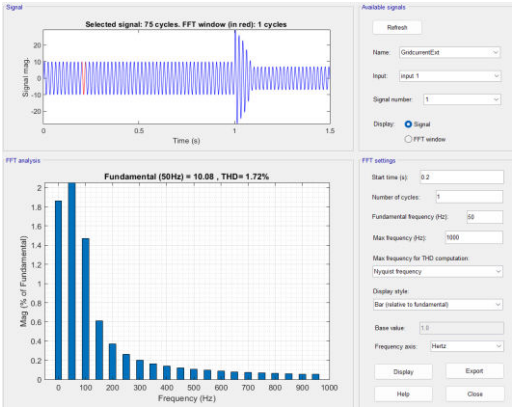

Fig.19 THD% Grid Current

The above fig .19 Shows Drastic reduction down to a highly clean 1.72%. Fundamental Magnitude (50Hz): The peak value increases 10.08.

COMPARISON TABLE

Parameter	PI Controller	FOPID Controller
Rise Time (Tr)	0.06 sec	0.015sec
Settling Time (Ts)	0.08sec	0.03sec
Overshoot (%)	10%	2%
Voltage Sag Compensation (%)	Restores to 94%	Restores to 97%
Voltage Swell Compensation (%)	Reduces to110%	Maintains102%
Load Variation Response Time	0.1 sec	0.04 sec
Steady-State Error	4 %	1 %
THD (Load Voltage)	18.91%	1.53 %
THD (Grid Current)	31.93%	1.72 %
Power Factor	0.96	0.99
System Stability Margin	Moderate	High
Controller Gain Sensitivity	High	Low
Robustness Index	Medium	High
Control Complexity	Low	Medium

CONCLUSION

This study presents a transformer less single-phase UPQC integrated with a standby converter module and regulated via an advanced FOPID controller to mitigate grid power quality issues. By implementing a load-independent decoupling technique and a hysteresis-based control strategy, the system operates at a high modulation index during nominal and sag conditions, activating the standby unit exclusively during voltage swells to maximize efficiency. This structural improvement lowers semiconductor blocking voltage stresses and optimizes passive components by significantly reducing inductor sizes, yielding a direct cost saving of $20. Ultimately, the integration of the FOPID controller provides superior robustness and faster transient responses compared to traditional PI variants, with simulation results validating the system's exceptional ability to suppress voltage sags, swells, and total harmonic distortion (THD).

REFERENCES

[1] H. Akagi, “New trends in active filters for power conditioning,” IEEE Trans. Ind. Appl., vol. 32, no. 6, pp. 1312–1322, Nov./Dec. 1996.

[2] B. Singh, K. Al-Haddad, and A. Chandra, “A review of active power filters for power quality improvement,” IEEE Trans. Ind. Electron., vol. 46, no. 5, pp. 960–971, Oct. 1999.

[3] V. Khadkikar, “Enhancing electric power quality using UPQC: A comprehensive overview,” IEEE Trans. Power Electron., vol. 27, no. 5, pp. 2284–2297, May 2012.

[4] A. Ghosh and G. Ledwich, Power Quality Enhancement Using Custom Power Devices. Boston, MA, USA: Kluwer, 2002.

[5] M. Kesler and E. Ozdemir, “A simplified control method for unified power quality conditioner,” IEEE Trans. Power Del., vol. 25, no. 4, pp. 2792–2800, Oct. 2010.

[6] J. M. Guerrero et al., “Hierarchical control of droop-controlled AC and DC microgrids,” IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 158–172, Jan. 2011.

[7] Y. Yang and F. Blaabjerg, “Overview of control strategies for grid-connected converters,” IEEE Trans. Ind. Appl., vol. 50, no. 5, pp. 3379–3393, Sept./Oct. 2014.

[8] I. Poddubny, "Fractional-order systems and PIλDμ controllers," IEEE Trans. Autom. Control, vol. 44, no. 1, pp. 208–214, Jan. 1999.

[9] C. A. Monje et al., Fractional-Order Systems and Controls: Fundamentals and Applications. London, U.K.: Springer, 2010.

[10] Y. Luo and Y. Chen, Fractional Order Motion Controls. Hoboken, NJ, USA: Wiley, 2012.

[11] S. Das, Functional Fractional Calculus for System Identification and Controls. Berlin, Germany: Springer, 2008.

[12] K. B. Mohanty and B. Subudhi, "FOPID controller design for power system applications," Int. J. Electr. Power Energy Syst., vol. 54, pp. 400–410, Jan. 2014.

[13] S. Panda and N. P. Padhy, "Optimal tuning of FOPID controllers using optimization techniques," Appl. Soft Comput., vol. 12, no. 2, pp. 563–572, Feb. 2012.

[14] X. Zhang, Y. Li, and Z. Chen, "Fractional-order control in power electronics systems," IEEE Trans. Power Electron., vol. 31, no. 7, pp. 5316–5326, July 2016.

[15] M. Karimi-Ghartemani and M. Iravani, "A method for synchronization of power electronic converters," IEEE Trans. Power Syst., vol. 19, no. 3, pp. 1263–1270, Aug. 2004.

[16] S. K. Jain, P. Agrawal, and H. O. Gupta, "Fuzzy logic controlled shunt active filter," IEEE Proc. Electr. Power Appl., vol. 149, no. 5, pp. 317–328, Sept. 2002.

[17] A. Bhattacharya, C. Chakraborty, and S. Bhattacharya, "Parallel-connected shunt active filters," IEEE Trans. Ind. Electron., vol. 50, no. 5, pp. 880–887, Oct. 2003.

[18] J. He and Y. W. Li, "Analysis and design of interfacing inverter for renewable systems," IEEE Trans. Power Electron., vol. 26, no. 10, pp. 2796–2807, Oct. 2011.

[19] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Grid synchronization techniques for power converters," IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1398–1409, Oct. 2006.

[20] B. Singh and V. Verma, "Selective compensation of power quality problems," IEEE Trans. Ind. Appl., vol. 45, no. 5, pp. 1969–1976, Sept./Oct. 2009.